AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

1. (Currently amended) A semiconductor device comprising:

a substrate; and

~~more than~~ at least three kinds of wells formed in and on a top surface of said substrate,

wherein at least one kind of well ~~from among the more than three kinds of wells~~ has a top surface height level higher than the top surface height levels of the other two kinds of wells in relation to the top surface of said substrate, ~~from among the more than three kinds of wells; said one kind of well is formed adjacent to and self-aligned to at least one kind of well from among said other kinds of wells; and~~ wherein said other two kinds of wells ~~are different in one of a~~ have a different conductivity type than said at least one kind of well~~, an impurity concentration and a junction depth, and include at least two kinds of wells having the same surface level~~.

2. (Currently amended) The semiconductor device as claimed in claim 1, wherein said other two kinds of wells have the same conductivity type and ~~include more than two kinds of wells having~~ have different impurity concentrations with relation to each other.

3. (Currently amended) The semiconductor device as claimed in claim 2, wherein at least one kind of well ~~from among said other kinds of wells~~ has an impurity concentration that is decreased to a level necessary to form a high-voltage transistor.

4. (Currently amended) The semiconductor device as claimed in claim 1, wherein said other two kinds of wells ~~include more than two kinds of wells having~~ have different junction depths within said substrate relative to each other.

5. (Currently amended) The semiconductor device as claimed in claim 4, wherein one of said other two kinds of wells ~~having~~ has a larger junction depth within said substrate and further includes a triple well in which a well of an opposite conductivity type having a smaller junction depth is formed.

6. (Currently amended) The semiconductor device as claimed in claim 1, wherein said at least one kind of ~~wells~~ well and said other two kind of wells are of different conductivity types to each other.

7. (Currently amended) The semiconductor device as claimed in claim 1, wherein a MOS transistor is formed by a drain diffusion layer and a source diffusion layer formed in the ~~more than~~ at least three kinds of wells and a gate electrode formed on areas corresponding to the drain diffusion layer and the source diffusion layer via a gate insulating film.

8. (Currently amended) The semiconductor device as claimed in claim 5, wherein MOS transistors are formed by drain diffusion layers and source diffusion layers formed in the ~~more than~~ at least three kinds of wells and gate electrodes formed on areas corresponding to the drain diffusion layers and the source diffusion layers via a gate insulating film, and wherein one of the MOS transistors formed on the triple well is one of a MOS transistor constituting a power supply circuit, a MOS transistor constituting a circuit sensitive to a substrate noise and a MOS transistor constituting a circuit generating a noise.

9. (Withdrawn) A manufacturing method of a semiconductor device having more than three kinds of wells in a single substrate, comprising the steps of:

(A) forming a first silicon nitride film on said substrate;

(B) forming a first resist pattern by a photolithography so as to define a first well area, removing a part of said first silicon nitride film corresponding to an opening of said first resist pattern by etching, introducing first impurity ions into said first well area of said substrate by ion implantation so as to form said first well area, and removing said first resist pattern;

(C) applying a heat treatment to said substrate within an oxidizing atmosphere so as to form a first thermal oxide film on an area of a surface of said substrate that is not covered by said first silicon nitride film and simultaneously diffuse the first impurity ions introduced into said substrate to form the first well;

(D) removing said first silicon nitride film, forming a second silicon nitride film on said substrate including said first thermal oxide film, forming a second resist pattern on said second silicon nitride film by a photolithography so as to form a second well area, removing a part of said second silicon nitride film corresponding to an opening of said second resist pattern by etching so as to define said second well area, introducing second impurity ions into said second well area of said substrate by ion implantation so as to form the second well, and removing said second resist pattern;

(E) applying a heat treatment to said substrate within an oxidizing atmosphere the same as said oxidizing atmosphere in the step (C) so as to form a second thermal oxide film on an area of a surface of said substrate that is not covered by said second silicon nitride film and simultaneously diffuse the second impurity ions introduced into said substrate to form the second well;

(F) removing said second silicon nitride film, and introducing third impurity ions into said substrate by using said first and second thermal oxide films as masks so as to form a third well area in a self-alignment manner; and

(G) applying a heat treatment to said substrate in a non-oxidizing atmosphere so as to diffuse the third impurity ions to form the third well.

10. (Withdrawn) The manufacturing method as claimed in claim 9, wherein the processes of steps (D) and (E) are repeated for a plurality of times while changing at least one of a kind of said second impurity ions, an amount of said second impurity ions to be introduced and an implantation condition of said second impurity ions.

11. (Withdrawn) A manufacturing method of a semiconductor device having more than three kinds of wells in a single substrate, comprising the steps of:

(A) forming a silicon nitride film on said substrate;

(B) forming a first resist pattern by a photolithography to define a first well area, removing a part of said silicon nitride film corresponding to an opening of said first resist pattern by etching, introducing first impurity ions into said first well area of said substrate by ion implantation so as to form said first well area, and removing said first resist pattern;

(C) forming a second resist pattern by a photolithography so as to form a second well area, removing a part of said silicon nitride film corresponding to an opening of said second resist pattern by etching so as to define said second well area, introducing second impurity ions into said second well area of said substrate by ion implantation so as to form the second well, and removing said second resist pattern;

(D) applying a heat treatment to said substrate within an oxidizing atmosphere so as to form a thermal oxide film on an area of a surface of said substrate that is not covered by said silicon nitride film and simultaneously diffuse the first and second impurity ions introduced into said substrate to form the first and second wells;

(E) removing said silicon nitride film, and introducing third impurity ions into said substrate by using said thermal oxide film as a mask so as to form a third well area in a self-alignment manner; and

(F) applying a heat treatment to said substrate in a non-oxidizing atmosphere so as to diffuse the third impurity ions to form the third well.

12. (Withdrawn) The manufacturing method as claimed in claim 11, wherein the step (B) includes a step of applying a heat treatment in a non-oxidizing atmosphere before proceeding to a subsequent ion implantation process.

13. (Withdrawn) The manufacturing method as claimed in claim 12, wherein the step (B) includes a step of applying a heat treatment to said substrate in an oxidizing atmosphere so as to form a protective oxide film on the surface of said substrate before applying the heat treatment in said non-oxidizing atmosphere.

14. (Withdrawn) The manufacturing method as claimed in claim 13, wherein said protective oxide film has a thickness in a range of 10 nm to 50 nm.

15. (Withdrawn) The manufacturing method as claimed in claim 11, wherein the process of step (B) is repeated for a plurality of times while changing at least one of a kind of said first impurity ions, an amount of said first impurity ions to be introduced and an implantation condition of said first impurity ions.

16. (Withdrawn) The manufacturing method as claimed in claim 11, further comprising a step of applying a heat treatment to said substrate in a non-oxidizing atmosphere after repeating the process of step (B) and before proceeding to a subsequent ion implantation process.

17. (Withdrawn) The manufacturing method as claimed in claim 16, further comprising a step of applying a heat treatment to said substrate in an oxidizing atmosphere so as to form a protective oxide film on the surface of said substrate before applying the heat treatment in said non-oxidizing atmosphere.

18. (Withdrawn) The manufacturing method as claimed in claim 17, wherein said protective oxide film has a thickness in a range of 10 nm to 50 nm.

19. (Withdrawn) The manufacturing method as claimed in claim 9, wherein a deeper well is formed earlier.

20. (Withdrawn) The manufacturing method as claimed in claim 9, further comprising a step of forming a third resist pattern within a specific well by a photolithography so as to define a triple well before applying the final heat treatment in said non-oxidizing atmosphere, introducing fourth impurity ions of a conductivity type opposite to said specific well into said substrate under a condition in which a depth of said triple well becomes shallower than said specific well, and removing said third resist pattern.

21. (Withdrawn) The manufacturing method as claimed in claim 9, wherein the final heat treatment in said non-oxidizing atmosphere is omitted so that the third impurity ions are diffused by a heat treatment applied when performing a field oxidation for element isolation.

22. (Withdrawn) The manufacturing method as claimed in claim 11, wherein a deeper well is formed earlier.

23. (Withdrawn) The manufacturing method as claimed in claim 11, further comprising a step of forming a third resist pattern within a specific well by a photolithography so as to define a triple well before applying the final heat treatment in said non-oxidizing atmosphere, introducing fourth impurity ions of a conductivity type opposite to said specific well into said substrate under a condition in which a depth of said triple well becomes shallower than said specific well, and removing said third resist pattern.

24. (Withdrawn) The manufacturing method as claimed in claim 11, wherein the final heat treatment in said non-oxidizing atmosphere is omitted so that the third impurity ions are diffused by a heat treatment applied when performing a field oxidation for element isolation.